

Foreign Comparative Test of Space Qualified Digital Signal Processors¹

Steven Sampson, Paul Duggan and Richard Burnell
Air Force Research Laboratory
Space Vehicles Directorate
3550 Aberdeen Avenue SE
Kirtland AFB, NM 87117-5776
505-846-5816
steven.sampson@kirtland.af.mil

Steven McEndree, Jake Tausch, David Sleeter and David Alexander
Mission Research Corporation
5001 Indian School Road NE
Albuquerque, NM 87110-3946
505-768-7684
mcendree@mrcmicroe.com

Rocky Koga, Paul Yu and Susan Crain
The Aerospace Corporation
2530 E El Segundo Blvd.
El Segundo, CA 90245-4691
310-336-6583
rokutaro.koga@aero.org

Abstract— The ADSP-21020 digital signal processor (DSP) was originally designed by Analog Devices Incorporated (ADI) for high performance audio and video signal processing functions in commercial applications. However, the same functionality is needed for military and space applications related to imaging and communications. Consequently, the original design was licensed to BAE Systems (formerly Lockheed Martin Space Electronics and Communications) [1] and Atmel Wireless and Microcontrollers (formerly Temic Semiconductors) [2] for the development of radiation tolerant versions. Both companies presently offer the radiation tolerant parts for applications in space and missile systems. However, each company targeted a slightly different market segment and their products have different radiation hardness levels. The two companies specify the radiation hardness levels differently, and neither provides information on ionizing dose rate performance. The purpose of the work described in this paper was to develop and implement a radiation test methodology to characterize parts from each vendor in a common set of environments. The goal was to obtain a uniform set of data to permit direct comparison of response among the commercial and radiation tolerant devices from each vendor.

The results reported here permit a comparison of 21020 DSPs from each of three vendors. Devices from ADI exhibit radiation response expected of non-hardened parts from commercial complementary metal oxide

semiconductor (CMOS) technologies, although their total ionizing dose (TID) hardness was somewhat better than expected. These commercial parts fail between 24 krad (Si) and 64 krad (Si). The BAE Systems parts showed no significant change in standby current and no functional failures up to a dose of 2 Mrad (Si), where the testing was stopped. The dose rate hardness was consistent with the extremely thin epitaxial layer used in their radiation hard technology. The single event effects (SEE) hardness of the BAE Systems parts was comparable to the commercial parts as expected since the storage elements were not hardened. The Atmel parts showed TID hardness in excess of their 100 krad (Si) specification even at the 100 rad (Si) per second dose rate. Their dose rate hardness fell between the commercial and BAE Systems devices, probably reflecting a relatively thick epitaxial layer. Their SEE hardness was quite good as a result of design hardening of the storage elements.

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I. INTRODUCTION

This Department of Defense (DoD) Foreign Comparative Test (FCT) funded project was sponsored by the Military Satellite Communications Advanced Extremely High Frequency (AEHF) joint program and National Polar-orbiting Operational Environmental Satellite System (NPOESS) integrated program offices. This project leverages non-developmental items of France and Austria to provide DSP products within these U.S. defense satellites more quickly and economically than the normal acquisition development process.

The FCT Project Goal

A French version of the ADSP-21020 DSP from Atmel and the Austrian Aerospace's Digital Receiver Processor Module (DRPM) were compared with the BAE Systems DSP and TRW's AEHF controller circuit board, respectively. The sponsoring U.S. defense satellite programs' interests gave radiation requirements to evaluate the target products. Each product's relative performance advantages led to future procurement potential during engineering manufacturing development of the sponsoring satellite systems.

This FCT project's goal is to reduce the acquisition cycle time and research, development, test and evaluation expenditures while enhancing standardization and interoperability with worldwide commercial manufacturing sources. This improves cooperation with foreign nations thus promoting competition while eliminating unnecessary duplication of technology solutions.

DSP Comparisons

A physical comparison of the three devices is shown in Figure 1. The ADI chip is shown on the left. The BAE Systems chip, the RH21020, is in the center, and the Atmel TSC21020F is on the right. The die are shown to scale. The ADI device is the smallest with the BAE Systems and the Atmel devices being a factor of 1.14 and 1.11 larger in area, respectively.

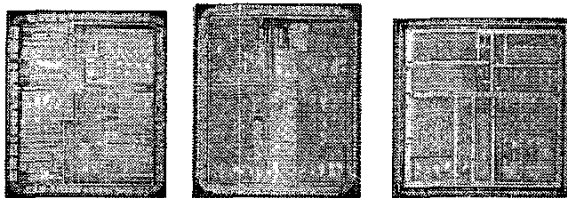


Figure 1. Die photographs for the ADI, BAE and Atmel 21020 vendor devices, respectively.

A common set of software was developed and run on each version of the DSP. The software exercised the major functional blocks and permitted both static and dynamic assessments of the device performance during irradiation.

The software was developed with commercially available support tools.

Test Configuration

The ADI, Atmel, and BAE Systems devices are all available in a 223 terminal, pin grid array (PGA) package. The Atmel and BAE Systems devices are also available in 256 pin, quad flat packs. For this project, both the Atmel devices and the BAE Systems devices were packaged in quad flat packs. The ADI devices were tested in a pin grid array. All testing was performed on socketed devices. The Atmel and BAE Systems devices were purchased as QML (Qualified Manufacturers' List) class Q devices. All testing was performed at 20 MHz, and at a supply voltage of 5.0 Volt. The ADI device specifies a range of operating frequencies, from 20 MHz to 33 MHz; the particular ADI devices we tested have an operating frequency of 20 MHz. The nominal operating frequency of the Atmel device is 20 MHz. The BAE Systems device specifies a maximum operating frequency of 25 MHz. All the 21020 DSPs operate at a nominal supply voltage of 5.0 Volt.

2. DEVICE LEVEL RADIATION TESTING

Figure 2 is a photograph of the test instrumentation used for both the TID and dose rate experiments. (A conceptually similar test set was used for SEE testing.) The test card assembly is shown in the upper left as configured for TID testing. The cabling on the left side of the board connects the 21020 to the PWS (Parametric Work Station) and ATV (Algorithmic Test Vector Generator). The PWS was used to measure parametric performance of input/output (I/O) terminals as a function of radiation. Current and voltage characteristics of the terminals for the high state, low state, and tri-state were recorded and compared with specified values to determine parametric failure thresholds.

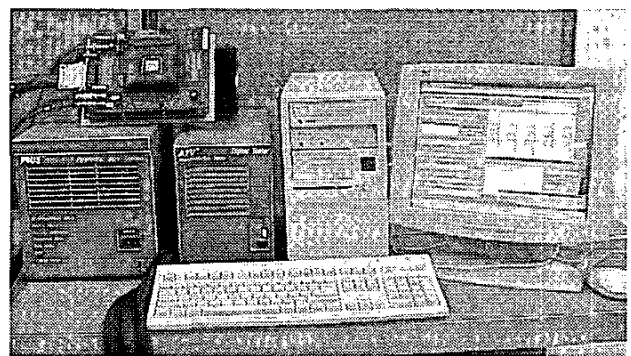


Figure 2. Test instrumentation for 21020 radiation testing.

The ATV was used to monitor functional performance. It initiated the execution of programs stored in electrically erasable programmable read only memory (EEPROM) and monitored the results of those programs to compare them with pre-irradiation values to determine when a functional failure threshold occurred. Both the ATV and PWS were

computer controlled with the Dynamic Test Environment (DTE) software. The DTE manages both the parametric and functional test data and stores the results in Excel-compatible files.

During testing, the control computer was always located in the instrumentation room. For TID testing, the PWS and ATV were also located in the instrumentation room, and the device under test (DUT) was checked for parametric and functional performance after each irradiation step. For dose rate testing, the ATV was lead brick shielded and located in the test cell so that the DUT could be exercised dynamically during the test. The ATV and the instrumentation cable were routed out of the beam to reduce noise.

The DUT board is shown in Figure 3 with an Atmel device in the test socket for a quad ceramic flat pack. A similar board with a socket for a pin grid array was used for the ADI device. The crystal oscillator can be seen as a white square shaped object in the upper left corner of the DUT board. It provided the clock for the device under test. During irradiation, it was shielded and closely monitored to ensure that it did not fail. Chip resistors used for loading the I/O terminals can be seen on each of the four sides of the DUT. Approximately 50% of standard inputs and outputs were pulled up to Vdd and 50% were pulled down to Vss during testing. For tri-state outputs, 25% were set to a high state, 25% were set to a low state, 25% were set to high impedance state and pulled up to Vdd, and 25% were set to high impedance state and pulled down to Vss.

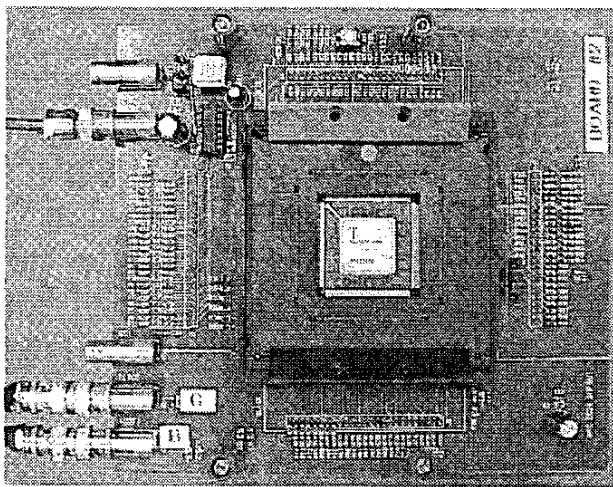


Figure 3. Photograph of the DUT board assembly.

All Vss connections for the 21020 were made to a local ground plane that was floated above the universal board ground with a 5 milliohm resistor. The voltage across the isolation resistor was used to monitor the total chip photocurrent during dose rate tests.

The EEPROM board is shown in Figure 4. The three EEPROMs used to store the 21020 programs are located to

the left of center with the white labels. Additional control and buffer logic is also located on the EEPROM board. The DUT card plugs into the EEPROM card via the four sockets, which position the device under test directly over the hole in the card. There is a matching hole in the DUT card beneath the 21020. These holes minimize the interaction between the board and the electron beam during dose rate testing to reduce replacement currents and associated noise.

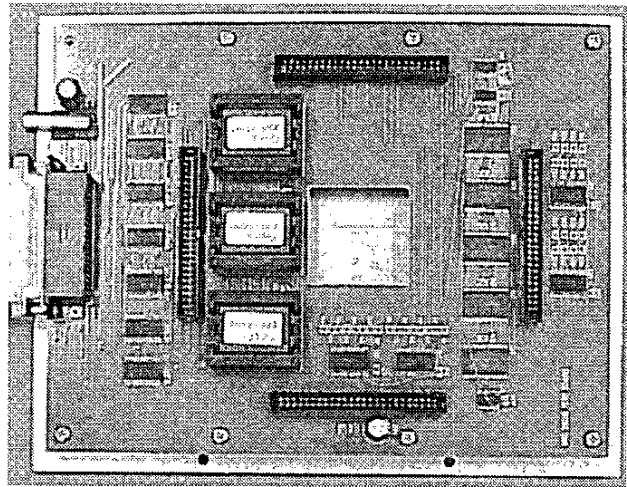


Figure 4. Photograph of the EEPROM board assembly.

For TID testing, the EEPROM card remained in the instrumentation room. A checkerboard pattern was loaded into the DUT registers, and the DUT card was detached from the EEPROM card. Bias was maintained with a battery pack, and the DUT was transported to the test cell; power then was supplied via a cable from the laboratory supply in the instrument room. After irradiation, the process was reversed, and the DUT was checked to determine if the pattern was still loaded.

In general, the test fixtures were designed to provide as much commonality as possible among the test configurations needed for the different radiation environments. This approach reduced the cost of fixturing and simplified the software development effort. The specific test procedures for each radiation environment are described in the following sections.

3. TID – HIGH DOSE RATE EFFECTS

TID characterization was performed at the Air Force Research Laboratory (AFRL) ⁶⁰Co source at a dose rate of 100 rad (Si)/s, as measured by a Rad-Cal 2025 ion-chamber dosimeter. The AFRL source is a panoramic room irradiator with an activity of 5,200 Ci. All irradiations were performed while the test devices were situated in a lead-aluminum box compliant with ASTM Standard E-1249. The size of the test cell allowed two test devices to be irradiated simultaneously. For these TID characterizations,

a total of ten devices were characterized: two of the ADI devices (in the 223 terminal pin grid array package), four of the BAE Systems devices, and four of the Atmel devices (both BAE Systems and Atmel in the 256-pin quad flat packs). Figure 5 shows the test setup for the ^{60}Co irradiation.

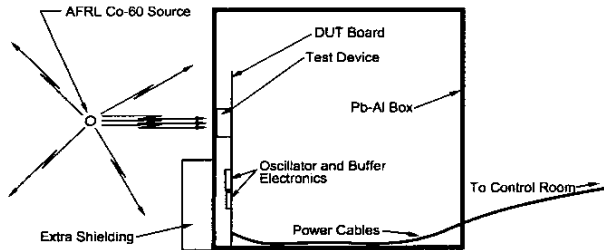


Figure 5. Test setup for TID irradiation.

The test devices were irradiated under 5.0 Volt bias and clocked at 20 MHz with a checkerboard pattern written into the register file. Following each exposure level, the devices were evaluated by running the following sequence of program tests:

1. Checker Board Test – A checkerboard pattern was read from the register array, errors were logged, the checkerboard was re-written, re-read, errors logged, and the supply current recorded. The checkerboard program determined if the pattern had been retained during irradiation and if the pattern could be rewritten.
2. Not Checker Board Test – An inverse checkerboard pattern was written into the register array and read to determine if the write was successful. The supply current was also recorded. This test was performed to determine if there was a significant increase in standby current when a pattern, complementary to that stored during irradiation, was written into the registers.
3. Arithmetic Logic Unit (ALU) Test – A series of mathematical operations was performed in the floating point ALU. This test was performed to check for timing changes resulting from TID exposure.
4. Null Operation (NOP) Tests – A series of loop operations was performed to check the functionality of external memory access circuitry.
5. Set Bias Tests – The final test was performed to check the ability to write a checker board pattern into the registers in preparation for the next irradiation event.

In addition to the functional tests, parametric values were measured and recorded for the supply current, logic high state voltage, logic low state voltage, and voltage for a tri-stated output pulled up to V_{dd}. The series of functional and parametric tests were conducted at 4.5 Volts, 5.0 Volts, and 5.5 Volts following each irradiation.

The results of the tests are summarized in the plots of supply current versus dose in Figure 6. The ADI (commercial) devices failed between 24 krad (Si) and 64 krad (Si). One device exhibited a multiplier timing error during a 4.5 Volt test at 24 krad (Si), although it passed at higher voltages. The second device remained fully functional at all voltages up to 64 krad (Si) when the not-checker board read pattern failed. Both units had supply currents that were out of specification at 64 krad (Si).

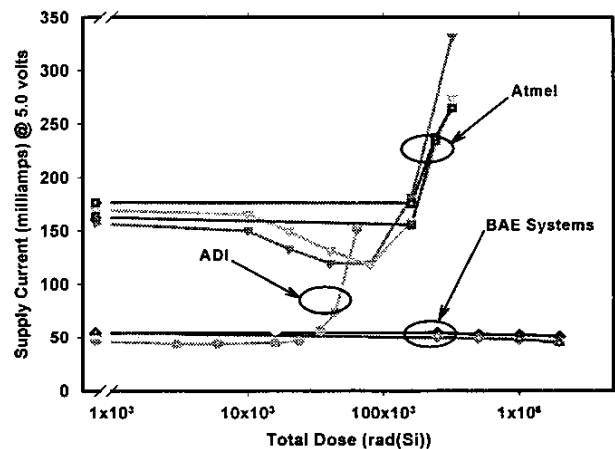


Figure 6. Supply current for 21020 devices from three vendors as a function of TID.

The Atmel devices showed a functional failure in the 4.5 Volt ALU test at 320 krad (Si). However, all four devices showed significant increases in supply current between 160 krad (Si) and 240 krad (Si) and exceeded specification at 240 krad (Si). In general, the Atmel devices operated with much higher standby currents than the devices from the other two vendors.

The BAE Systems devices showed no significant change in standby current and no functional failures up to a dose of 2 Mrad (Si), where the testing was stopped.

As shown in Figure 7, both the commercial ADI device and the Atmel devices exhibited significant annealing after 168 hours at 100 °C. The post-anneal supply current was actually lower than the pre-rad values for the Atmel devices. As indicated in the figure, one of the Atmel devices was annealed at room temperature for 168 hours. It also showed significant annealing although not as large as the devices subjected to high temperature.

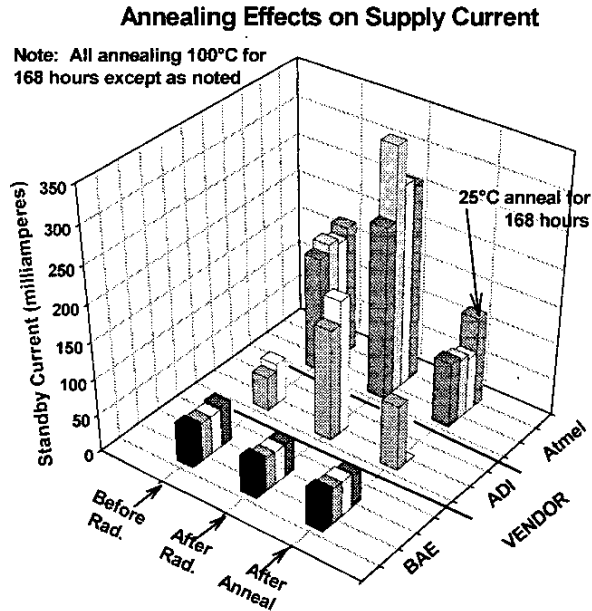


Figure 7. Comparison of supply currents.

4. TID - LOW DOSE RATE EFFECTS

At the conclusion of the TID evaluation in the ^{60}Co source, the low dose rate TID evaluation was begun. This was performed using the AFRL ^{137}Cs source, and, as for the ^{60}Co TID evaluation, the test device was placed in a lead-aluminum box compliant with ASTM Standard E-1249. The limited size of the test cell allows testing of only one device at a time. The dose rate at the test device was measured with the Rad-Cal 2025 dosimeter to be 0.0123 rad (Si)/sec, or approximately 1062 rad (Si)/day. Due to the time required for low dose rate tests when only one device could be tested, the test team decided to evaluate Atmel devices in the low dose rate environment. This is because the test team determined that the BAE Systems devices would probably show no trapped charge in the oxide response at the low dose rate exposures to reach their much (ten times) higher specified failure level. The Atmel devices had also been previously tested and specified by Atmel in a low dose rate environment up to a much (ten times) lower specified failure level which could be easier to achieve. As this report is being written, the first Atmel device is undergoing the low dose rate irradiation and evaluation. Figure 8 shows the setup for the low dose rate irradiation.

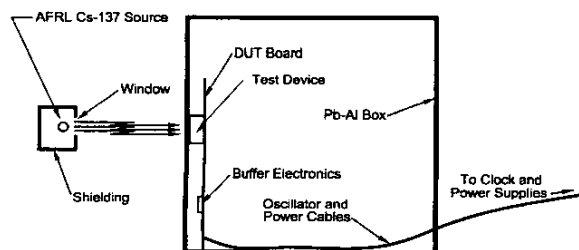


Figure 8. Test setup for low dose rate TID irradiation. As was the case for the ^{60}Co TID testing, the test devices were irradiated under 5.0 Volt bias and clocked at 20 MHz with a checkerboard pattern written into the register file. Following each exposure level, the devices were evaluated by running the same sequence of program tests as for the ^{60}Co testing. These include the Checker Board test, the Not Checker Board test, the ALU test, the NOP test, and the Set Bias test. Also, the same parametric values were measured and recorded. The functional and parametric tests were conducted at supply voltages of 4.5, 5.0, and 5.5 Volts.

The results of the low dose rate evaluation are summarized in the plot of supply current versus TID in Figure 9. It should be noted that Figure 9 shows partial data for a single test device. The Atmel device still being irradiated showed no functional failures, and no significant change in the parametric measurements to a TID of 116 krad (Si). Thus far, the supply current has decreased slightly with increasing TID.

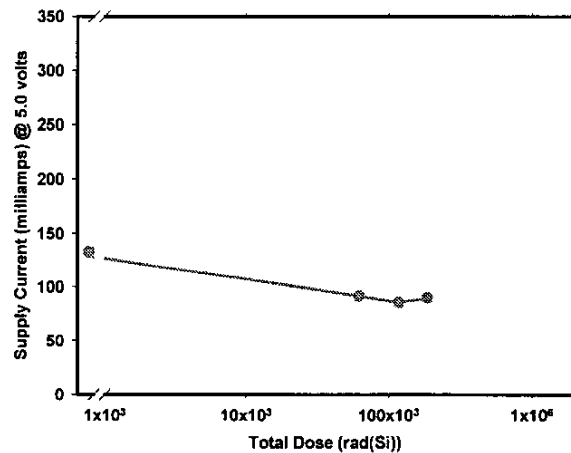


Figure 9. Supply Current for Atmel 21020 device #LD01 as a function of TID - low dose rate.

5. IONIZING DOSE RATE EFFECTS

Ionizing dose rate testing of the 21020 digital signal processor devices from ADI, BAE Systems, and Atmel was performed at the Little Mountain linear accelerator (LINAC) facility at Hill Air Force Base, Utah. Upset, latchup, and burnout tests were completed on four devices each from the Atmel and BAE Systems samples and on one device from ADI. The upset evaluation included tests to determine (1) transient parametric upset on the output channels, (2) static memory and register file upset, and (3) dynamic upset threshold for random access memory (RAM) and register operations, central processor unit (CPU) intensive operations, ALU intensive operations, program counter intensive operations, and branch intensive operations under realistic operating conditions. All tests were performed with an input clock rate of 20 MHz. Upset tests were performed with a 5 Volt power supply at room temperature. Latchup and burnout tests were performed

with a 5.5 Volt power supply at 100°C case temperature. No latchup or burnout were observed for any of the devices.

Table 1 is a summary of the upset test results. The values in the table represent the lowest upset threshold for each device at each test condition. The parametric upset column records the dose rate at which the output waveform transient exceeded 1/3 of the specified voltage range between V_{OH} (high state output voltage) and V_{OL} (low state output voltage). As expected the commercial devices from ADI exhibited the lowest upset thresholds. In general, they could not be reliably used above a dose rate of approximately $1.0E8$ rad (Si)/s. The Atmel devices could be used up to $5.0E8$ rad (Si)/s, and the BAE Systems devices could be used to $1.0E9$ rad (Si)/s.

The relative dose rate hardness for the three device types is also reflected in their photocurrent response. Figure 10 is a graph of the peak photocurrent for a typical device from each manufacturer.

As shown in Figure 10, the photocurrents for the ADI device as measured at the V_{SS} terminal were much larger than those for either the Atmel or the BAE devices. The ADI photocurrents also exhibited a much longer decay time. Taken together these indicate that the ADI devices were either fabricated on a non-epitaxial substrate or that the substrate layer was very thick. The Atmel devices exhibited a consistently larger photocurrent than the BAE devices, although the waveshapes were similar for each device type and essentially followed the radiation pulse.

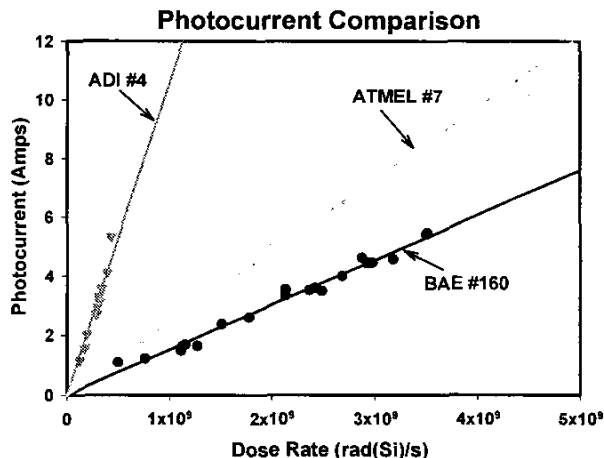


Figure 10. Peak photocurrent for a typical device from each manufacturer.

This indicates that both devices were fabricated on an epitaxial substrate. The BAE substrate was much thinner in keeping with their normal processing practices [3]. In general, the photocurrent measurements were consistent with the observed upset thresholds.

6. SINGLE EVENT EFFECTS

Single event effects testing of the Atmel and BAE Systems devices was carried out at the Lawrence Berkeley Laboratory 88-inch cyclotron facility. Ions with linear energy transfer (LET) values of 2.0, 3.2, 9.8, 21.9, 29.6 and 53.7 MeV-cm²/mg were used. The configuration of the test hardware for the SEE testing is shown in Figure 11. The test devices exercise in vacuum as heavy ion irradiation occurs.

Serial Number	Parametric Upset rad(Si)/s	Static Upset rad(Si)/s	Static Upset Condition	Dynamic RAM/Reg. Upset rad(Si)/s	Dynamic RAM/Reg. Upset Condition	Dynamic CPU Upset rad(Si)/s	Dynamic CPU Upset Condition	Dynamic ALU Upset rad(Si)/s	Program Counter Upset rad(Si)/s	Branch Upset rad(Si)/s
ADI #4	1.95 E8	1.49 E8	Lonely 1	3.37 E8	RAM Write	2.62 E8	Read Upset	1.95 E8	3.46 E8	2.97 E8
BAE #160	1.51 E9	2.68 E9	Lonely 1	1.13 E9	Reg Read			1.11 E9	2.36 E9	2.13 E9
BAE #170	1.69 E9	2.50 E9	Checker board	2.43 E9	RAM Write	3.07 E9	RAM Write	2.59 E9	2.90 E9	2.05 E9
BAE #171	1.74 E9	2.50 E9	Lonely 0	2.16 E9	Reg Write	3.51 E9	Reg Write	2.19 E9	2.69 E9	2.25 E9
BAE #172	1.50 E9	2.41 E9	Checker board	2.35 E9	RAM Write	2.78 E9	RAM Read		2.66 E9	2.84 E9
ATMEL #06	1.03 E9	2.03 E9	Lonely 0	5.64 E8	Reg Read			5.87 E8	1.58 E9	1.57 E9
ATMEL #07	1.15 E9	2.31 E9	Lonely 0	5.36 E8	RAM Read			6.43 E8	1.54 E9	1.53 E9
ATMEL #08	9.84 E8	2.00 E9	Lonely 0	5.98 E8	Reg Read			5.74 E8	1.45 E9	1.59 E9
ATMEL #09	8.64 E8	2.00 E9	Lonely 0	7.78 E8	RAM Read	2.05 E9	RAM Write	6.35 E8	1.57 E9	1.61 E9

Table 1. Summary of Dose Rate Upset Threshold for 21020 Digital Signal Processors

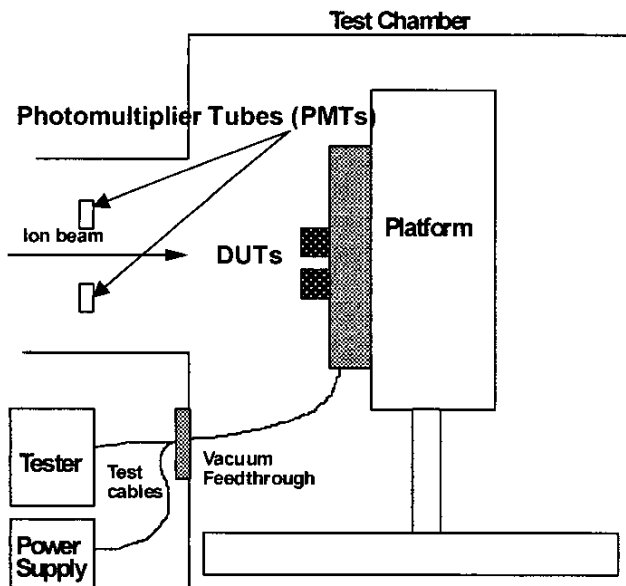


Figure 11. Test hardware configuration for SEE testing.

The test setup is shown in Figure 12. The Bus Access Storage and Comparison System (BASACS) is a "home made" logic analyzer test system which interfaces to a computer, and which is used to test various types of digital signal processors. BASACS can record the correct output signature of a DUT while the DUT is not in the beam line. Then it compares the DUT outputs with the recorded signature during exposure to a particle beam. This technique is called the "virtual golden chip" method. If the real "golden chip" method were used, the outputs of one device under beam would have been compared with those of another device ("golden chip") running at the same time outside of the beam. When a "golden chip" is replaced by a memory (storing the correct output signature), it becomes a "virtual golden chip". The record of correct output can be accumulated during a dry run without a beam. It can then be transferred and stored in the computer for future testing of that particular DUT.

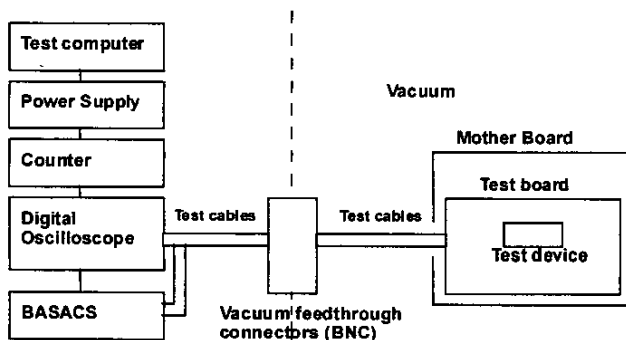


Figure 12. Test setup for SEE testing.

Four different software routines were used to exercise the devices during testing. In general, the BAE Systems

devices exhibited an LET threshold near 5 MeV-cm²/mg, while the devices fabricated by Atmel showed a very gradual decline in the upset cross-section starting from an LET value around 160 MeV-cm²/mg down to 30 MeV-cm²/mg. Weibull curves from the multiplier and shifter (MUL) program tests for each of the vendors' devices are shown in Figure 13 together with data on commercial ADI devices previously reported by BAE Systems [3]. The MUL program continuously exercises various multiplication and shifting operations in the processor. The internal processor cache memory is enabled during the execution of the MUL program. MUL program flowchart is shown in Figure 14.

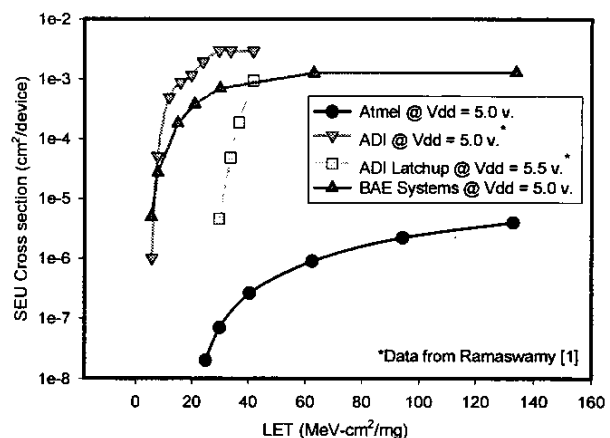


Figure 13. Comparison of SEU performance.

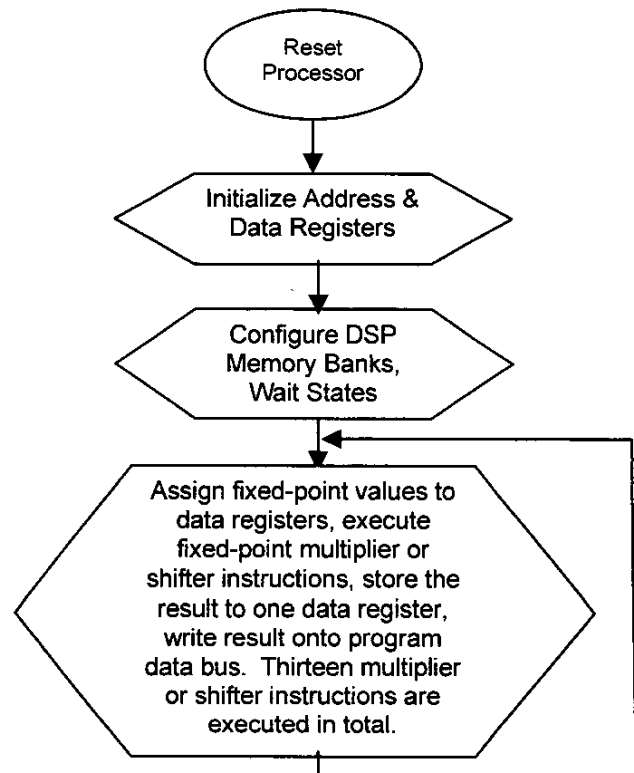


Figure 14. Flow diagram for MUL Program

7. BOARD LEVEL RADIATION TEST PLAN

Due to the prototype status of the DSP circuit boards used by the AEHF and NPOESS program offices, limited radiation test suites could be planned for each product. The AEHF circuit board contained only commercial unhardened electronic devices. The NPOESS circuit board contained radiation tolerant electronic devices. It was decided that only prompt dose upset test data would be of practical use for the AEHF program since any amount of TID would destroy board components. However, the NPOESS board was suitable for SEE testing as well as exposures to TID environments.

TRW AEHF Controller Board

This circuit board, developed under their Engineering Model (EM) contract for the AEHF program, is shown in Figure 15 containing two reverse-mounted ADSP-21020s. The DSP board was exposed to prompt dose radiation at the Hill Air Force Base UT LINAC. Ionizing dose rate levels captured operation during suspected DSP upset levels included in Table 1. Localizing the LINAC effects onto the Atmel or BAE Systems DSPs while isolating the entire circuit board required extreme care. A translation fixture facilitated exchanging master DSPs on the circuit board between test exposures. Two DSPs, a master and an auxiliary, reside on this controller board. Only master DSP (right hand vacant square on board) testing occurred due to physical LINAC orientation limitations. A Viterbi encoder/decoder algorithm also developed under the EM contract exercised most of the DSP functions. A timing flag bit synchronized the start/stop of the algorithm so that LINAC pulses could be identified as disrupting particular functions during execution.

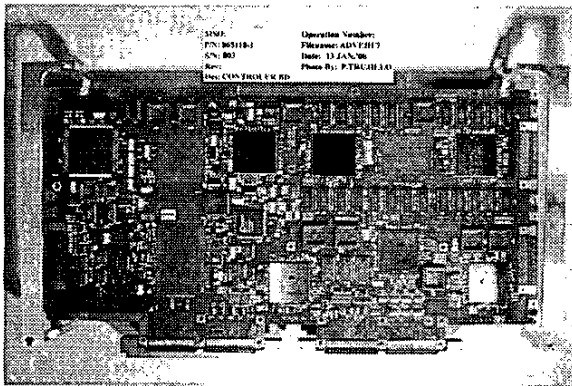


Figure 15. TRW AEHF Controller Board

Austrian Aerospace NPOESS DRPM

The Austrian Aerospace DRPM shown in Figure 16 was designed to function with a Global Positioning System Occultation Sensor planned for use by the NPOESS. SEE testing occurred at the Lawrence Berkeley Laboratory 88-inch cyclotron facility. Board level tests included similar

ion species and energy levels used during previous exposures of the individual Atmel and BAE Systems DSPs. The DRPMs were manufactured with an integral DSP adapter socket to facilitate DSP exchanges for consecutive exposures. Proprietary Austrian Aerospace test software was used to exercise the board during the exposures. Since multiple DRPMs were available, a "golden chip" test philosophy described earlier in this paper was applied and used to compare each DSP's upset characteristics.

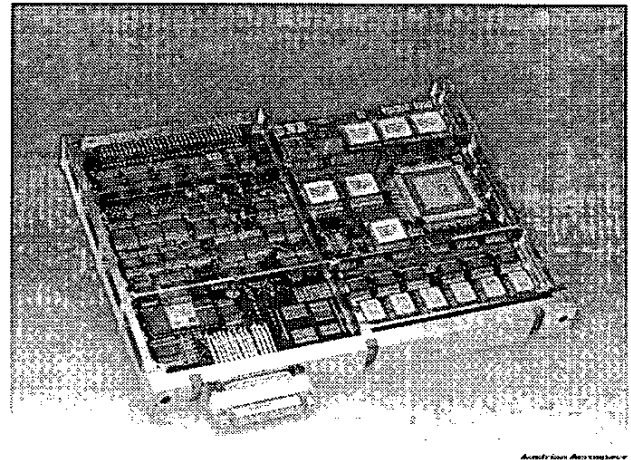


Figure 16. Austrian Aerospace DRPM Board

Limited size of the TID – low dose rate test cell permitted only high dose rate TID effects testing with the DRPM. The Air Force Research Laboratory (AFRL) ⁶⁰Co source used for testing provided a dose rate of 100 rad (Si)/s. Two DRPMs, one with an Atmel device another with a BAE Systems DSP, were exposed to radiation within a Pb-Al shielded box as specified in ASTM Standard E-1249. The proprietary Austrian Aerospace test software was once again used to exercise and functionally test the DRPM operation during irradiation. Failures that occur on the two different DSP populated DPRMs were defined at the radiation level that a specific electronic component contributed to intermittent or no further circuit board operations.

8. CONCLUSIONS

The results reported here permit a comparison of 21020 DSPs from each of three vendors. Devices from ADI exhibit radiation response expected of non-hardened devices from commercial CMOS technologies, although their TID hardness was somewhat better than expected.

The BAE Systems devices showed excellent TID hardness. The dose rate hardness was consistent with the extremely thin epitaxial layer used in their radiation hard technology. The SEE hardness of the BAE Systems devices was comparable to the commercial devices as expected since the storage elements were not hardened.

The Atmel devices showed TID hardness in excess of their 100 krad (Si) specification even at the 100 rad (Si)/s dose rate. Their dose rate hardness fell between the commercial and BAE Systems devices, probably reflecting a relatively thick epitaxial layer. The SEE hardness of the Atmel devices was quite good as a result of design hardening of the storage elements.

The first DSP circuit board radiation test data analysis results and preliminary performance estimates were provided to the respective manufacturers and satellite program offices. A final FCT report can be obtained from AFRL or the DoD FCT program office. Production of these foreign products now provides the demonstrated radiation resilience required for future defense satellites.

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Steven Sampson is a senior test and evaluation electronics engineer at Air Force Research Laboratory, Space Vehicles Directorate, Kirtland Air Force Base, New Mexico. He is primarily responsible for developing digital and analog signal processing electronics used in space and missile systems. He attained a Bachelor of Electrical Engineering degree with distinction from the University of Minnesota and a Master of Science in Electrical Engineering from New Mexico State University.



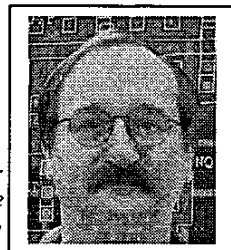
Paul Duggan is a Microelectronics Test Engineer at the Air Force Research Laboratory, Space Vehicles Directorate, Kirtland Air Force Base, New Mexico. He is responsible for planning and executing radiation effects testing on advanced microelectronics developed for Air Force and other DoD programs. He has received a Bachelor of Science in Electrical Engineering degree from the University of New Mexico.



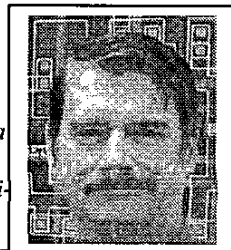
Richard Burnell is a program manager at the Air Force Research Laboratory, Space Vehicles Directorate, Kirtland Air Force Base, New Mexico. His programs include contracts such as Single Chip GPS Receiver, a Foreign Comparative Test project comparing digital signal processors, and developing a radiation tolerant 32-bit reduced instruction set computer. He attained a Bachelor of Physics degree followed by a Master of Science in Applied Physics degree at Northern Illinois University.



Steven McEndree joined Mission Research Corporation, Microelectronics Division in 2000, where he has been involved in electronics design and testing for radiation hardened environments. He received a Bachelor of Science degree in Electrical Engineering at New Mexico State University in 1982.



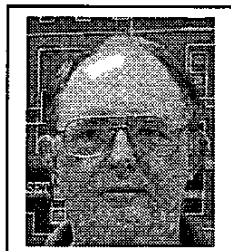
Jake Tausch joined Mission Research Corporation in 1991. He dedicated his career to designing and building specialized electronic test equipment. He received a Bachelor of Science degree in Electrical Engineering from the United States Air Force Academy in 1969 and a Master of Science degree in Electrical Engineering from the University of New Mexico in 1973.



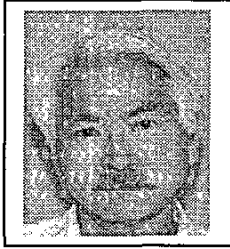
David Sleeter joined Mission Research Corporation in 1987 where he worked in the field of radiation effects and hardening of microelectronics and the design and building of specialized electronic test equipment. He received a Bachelor of Science degree in Electrical Engineering from the University of New Mexico in 1981.



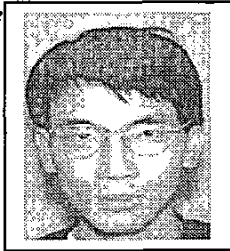
David Alexander joined Mission Research Corporation, in 1981, where he conducts research and development related to nuclear and space radiation effects on microelectronics. He received a Bachelor of Science in Electrical Engineering degree from the United States Air Force Academy in 1968 and a Master of Science in Electrical Engineering degree from the University of New Mexico in 1973.



Rocky Koga is a Distinguished Scientist at The Aerospace Corporation, where he has been working in the radiation effects area for twenty years. He earned a PhD degree in Physics from the University of California. He is a member of the Institute Electrical and Electronics Engineers.



Paul Yu is an Engineer with The Aerospace Corporation, where he has been working in radiation effects research for five years. He has a Bachelor of Science degree in Electrical Engineering from the University of Southern California.



Susan Crain is a senior engineer with The Aerospace Corporation, and has worked in the radiation effects area for seven years. She received a Bachelor of Science degree in Electrical Engineering from California State University. She is a member of the Institute Electrical and Electronics Engineers.

